Spring 2011
ESE 218: Digital Systems Design

Instructor: Dmitri Donetski, E-mail: dima@ece.sunysb.edu
Office Hours: Monday, Wednesday, 4:30 - 6:30 PM, 247 Light Eng. bldg.
Http://www.ece.sunysb.edu/~dima/ese218.html

Prerequisite: Engineering Major: PHY 127 or 132 or 142, or ESE 124
Computer Science Major: CSE 220

Description: The course develops methods of analysis and design of both combinational and sequential systems regarding digital circuits as functional blocks. The laboratory projects consist of simulation of digital circuits using CAD tools and building the circuits on breadboards.

Goal: Development of general background necessary for taking advanced Electrical and Computer Engineering courses.

Lectures: 079 Earth & Space Science, Tuesday, Thursday, 5:20 - 6:40 PM

Labs: 283A Light Eng. Bldg,
Section 1, Monday, 9:25 AM - 12:25 PM
Section 2, Monday, 6:55 PM - 9:55 PM
Section 3, Tuesday, 6:50 PM - 9:50 PM

Textbook (required): M. Morris Mano, Michael D. Ciletti, "Digital Design", 4rd ed., Prentice Hall, 2007, ISBN 0-13-198924-3

Lab kit (required): "ESE218", SUNYSB Bookstore

Grading: 11 homeworks (11 pts), 9 quizzes (9 pts), lab reports (15 pts), test 1 (15 pts), test 2 (20 pts), final exam (25 points), portfolio (5 points)

Topical outline:

1. Digital Concepts and Number Systems	Digital signals, binary number representations, Boolean switching algebra.	20%
2. Principles of Combinational Logic Design	Analysis and design of combinational logic, logic minimization, logic transformation.	30%
3. Principles of Sequential Logic Design	Flip-flops, counters, and registers. Finite state machines, sequential circuit design	50%

References:

1. Morris Mano, Charles Kime, "Logic and computer design fundamentals", Prentice Hall, 2004, ISBN 0-13-140539-X
2. Alan Markovitz, "Introduction to logic design", McGraw-Hill, 2005, ISBN 0-07-286516-4
3. John Wakerly, "Digital Design: principles and practices", Prentice Hall, 2006, ISBN 0-13-186389-4
4. William Kleitz, "Digital Electronics: a practical approach", Prentice Hall, 2002, ISBN 0-13-089629-2

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Any suspected instance of academic dishonesty will be reported to the Academic Judiciary. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/uaa/academicjudiciary/

Tentative Schedule:

Wk	Tuesdays HW due	Thursdays Quizzes	Topics	Labs	Textbook reading
1	Lect.1 2/1	Lect.2 2/3	Binary numbers and codes. Binary arithmetic. Logic operations and gates.	No lab	Ch.1, pp. 1-30
2	HW 1 Lect.3 2/8	Quiz 1 Lect.4 2/10	Error detection and correction. Boolean algebra. Digital logic families. Propagation delay.	No lab	Ch.2, pp. 36-64 Ch.10, pp. 471-508
3	HW 2 Lect.5 2/15	Quiz 2 Lect.6 2/17	Canonical and standard forms. Two-level implementations.	Lab 1 Board and Logic analyzer, Propagation delay	Ch.3, pp. 70-86 Ch.9, pp. 452-454
4	HW 3 Lect.7 2/22	Quiz 3 Lect.8 2/24	Logic maps and minimization. Incompletely specified functions. Introduction to HDL.	Lab 2 Algebraic manipulations	Ch.3, pp. 86-116
5	HW 4 Lect.9 3/1	**Test 1 3/3**	Review	Lab 3 Two-level implementations	Chapters 1-3
6	Lect.10 3/8	Lect.11 3/10	Adders, subtractors and comparators	Lab 4 Code converter	Ch.4, pp. 122-145
7	HW 5 Lect.12 3/15	Quiz 4 Lect.13 3/17	Decoders, encoders and multiplexer	Lab 5 Adder/subtractor	Ch.4, pp. 145-174
8	HW 6 Lect.14 3/22	Quiz 5 Lect.15 3/24	Latches and flip-flops. Analysis of sequential circuits	Lab 6 Decoders	Ch.5, pp. 182-220 Ch.9, pp. 422-432
9	HW 7 Lect.16 3/29	Quiz 6 Lect.17 3/31	Mealy and Moore outputs. Design of FSM with D-, T- and JK-flip-flops.	Lab 7 Design with multiplexers	Ch.5, pp. 182-234
10	HW 8 Lect.18 4/5	Quiz 7 Lect. 19 4/7	Synchronous counters. Multimode counters. Design of counters with D-, T- and JK flip-flops	Lab 8 State elements	Ch.6, pp. 258-265
11	HW 9 Lect.20 4/12	**Test 2 4/14**	Review.	Lab 9 Counters	Ch.6, pp. 242-253
12			**Spring Break 4/18-4/24**		
13	Lect.21 4/26	Lect.22 4/29	Registers. Shift registers. Ring and Johnson counters. Binary multipliers	Lab 10 Serial data transfer	Ch.6, pp. 265-269 Ch.8, pp. 371-382
14	HW10 Lect.23 5/3	Quiz 8 Lecture 24 5/5	Asynchronuous circuits, ripple counters. Synchronous FSM design practices	Lab 11 Sequential multiplier	Ch.6, pp. 253-258, Ch.9, pp.422-432
15	HW11 Lect 25 5/10	Quiz 9 Lect.26 5/12	State assignment and reduction. RAM, ROM, PAL, PLA PLD, CPLD, FPGA	Lab 11 Sequential multiplier (cont.)	Ch.5, pp. 221-225, Ch.9, pp. 439-442 Ch.7, pp. 284-328
Final Exam					